Design & Implementation of D Flip-Flop with Synchronous Reset using 90 nm technology

Prottay Barua
Dept. of Electrical and Electronic Engineering
Chittagong University of Engineering and Technology
Chittagong, Bangladesh
prottaybarua@yahoo.com

Prasun Mazumder
Dept. of Electrical and Electronic Engineering
Chittagong University of Engineering and Technology
Chittagong, Bangladesh
prasunmazumder562@gmail.com

***Abstract*— Flip flops are essential in digital circuits for data storage and synchronization. Adding synchronous reset enhances reliability by enabling controlled data clearing. Designed in standard CMOS technology, our D flip flop integrates logic gates and feedback loops for stable operation. Reset occurs synchronously with external clock cycles. Simulations and analysis validate setup time, hold time, propagation delay, and power consumption against benchmarks, affirming robust performance. Investigations into input conditions and clock frequencies highlight design stability. This research advances digital circuitry, demonstrating synchronous reset's benefits in achieving reliable data storage and controlled resetting, essential for integrated and efficient digital systems. This study focuses on the design and validation of a D flip-flop with synchronous reset, leveraging standard CMOS technology and Cadence Virtuoso tools.**

***Keywords*— D flip flop, synchronous reset, digital circuits, sequential logic, memory elements, data storage, clocked output, stability, design principles, operation, performance characteristics, simulations, digital systems.**

I. INTRODUCTION

Digital circuits form the backbone of modern computing systems, responsible for crucial tasks such as data storage, processing, and control. At the heart of these circuits lie flip flops, essential components that store and synchronize binary data within sequential logic circuits, memory units, and state machines [1].

Traditionally, flip flops have been fundamental in their design, primarily offering basic functionalities such as data storage and clocked output. However, as digital systems grow in complexity and sophistication, there arises a pressing need for more advanced features to enhance reliability, flexibility, and efficiency [2]. One such advanced feature is the inclusion of synchronous reset capability in flip flops.

Synchronous reset in a flip flop ensures that the stored data can be cleared or reset synchronously with a clock signal, typically on specific clock cycles. This capability is crucial in applications where precise control over data retention and reset operations is paramount. By synchronizing reset actions with the clock, it prevents unintended resets and ensures data integrity during critical operations [3].

The integration of synchronous reset enhances the overall reliability and stability of digital circuits, particularly in environments where accurate timing and data consistency are essential. It facilitates controlled resetting of flip flop states, which is vital in applications ranging from microprocessor design to communication protocols and digital signal processing [4].

In this context, this paper presents a comprehensive exploration of the design, implementation, and analysis of a D flip flop with synchronous reset. The objective is to delve into the theoretical foundations, design considerations, and performance evaluations of such a flip flop [5]. Through rigorous simulations and theoretical insights, this study aims to demonstrate the effectiveness and applicability of synchronous reset in enhancing the functionality and reliability of flip flops for modern digital circuit designs.

II. METHODOLOGY

To investigate the performance of a D flip-flop with synchronous reset using Cadence Virtuoso, we followed a structured methodology encompassing transient response, propagation delay, average power consumption, input noise, and output noise, culminating in the layout design [6].

First, We designed the gate level & transistor level schematic of D flip flop in Cadence Virtuoso. For transient response analysis, we established a test bench in the Virtuoso Analog Design Environment (ADE), applying clock, data, and reset signals to capture and examine the output waveforms, ensuring correct functionality. Propagation delay was measured by determining the time difference between the clock edge and the output change for data-to-Q delays, ensuring they met the design specifications. Average power consumption was analyzed using the ADE's power analysis tools. Input and output noise were evaluated by injecting noise into the input signals and observing the effect on the output using Virtuoso's noise analysis tools. Finally, the layout design was completed in Virtuoso Layout Suite, considering DRC & LVS test.

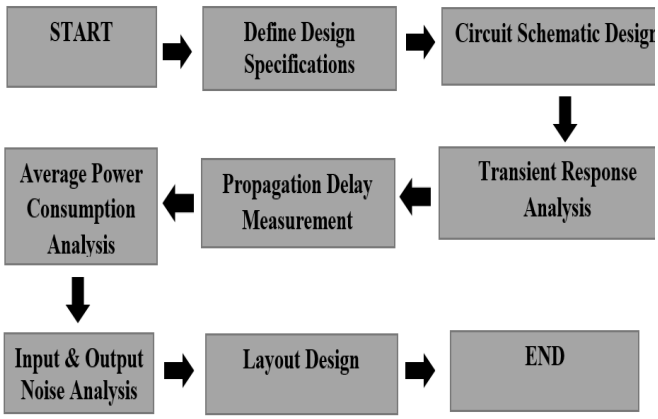

Fig. 1. Work flow diagram

III. Design Specifications

A. Equipments Used

The design of a D flip-flop with synchronous reset involves several essential components and equipment.

- It utilizes seven NAND gates for the primary logic operations, enabling the flip-flop to store and synchronize data based on the input conditions.
- Seven pins are employed for input and output connections, facilitating the interaction of signals with external components or other parts of the circuit.
- Wires are crucial for interconnecting these components according to the circuit layout design.
- A stable voltage source powers the flip-flop, ensuring consistent operation, while a ground connection completes the electrical circuit and provides a reference point for signal return paths.

Together, these components enable the implementation of a reliable D flip-flop with synchronous reset, essential in digital circuitry for controlled data storage and synchronization applications.

B. Design Parameters

To design the schematic of the D flip flop-

For the ground -

- voltage is 0 volt

For the Vdd-

- voltage is 1.2 volt.

For the Reset input-

- Voltage is 1.2 Volt.
- Period is 100 ms.
- Pulse Width 50 ms.

For the data input-

- Voltage is 1.2 Volt.
- Period is 40ms.
- Pulse Width 20 ms.

For the clock input-

- Voltage is 1.2 Volt.
- Period is 20ms.
- Pulse Width 10ms .

IV. Circuit Schematic Design

A. Operating Principle

The working principle of a synchronous D flipflop is simple It just follow the clock rising edge. When the reset signal is high the output follows the input in this time the clock has to have a positive edge. If the reset signal is low, the output will not change until it get the next positive edge of the clock signal [7]. The truth table of the synchronous D flip flop is-

TABLE I. Truth Table Of D Flip Flop

Input			Output	
D	Reset	Clock	Q	Q’
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

B. Gate Level Schematic Design:

Gate-level schematic design for a D flip-flop with synchronous reset involves constructing logic gates and sequential elements to implement a circuit that stores data on a clock edge while synchronously resetting based on another control signal [8].

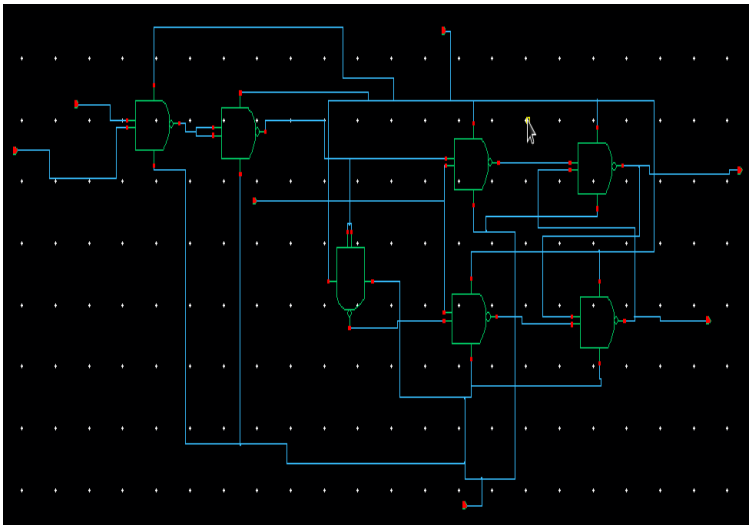

Fig. 2. Gate Level schematic design

C. Transistor Level Design:

Transistor-level schematic design for a D flip-flop with synchronous reset involves configuring MOSFET transistors

to create a circuit that stores binary data on a clock edge while synchronously resetting based on a control signal [9].

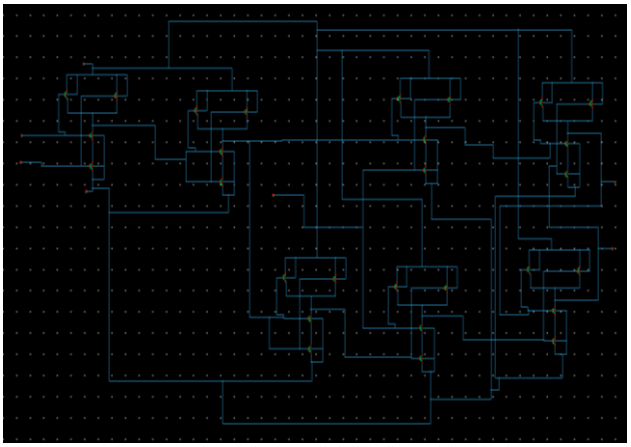

Fig. 3. Transistor level design of d flip flop with synchronous reset

D. Symbol:

Symbol for a D flip-flop with synchronous reset: a standard D flip-flop symbol with an additional reset input synchronized to the clock signal for resetting the flip-flop's state.

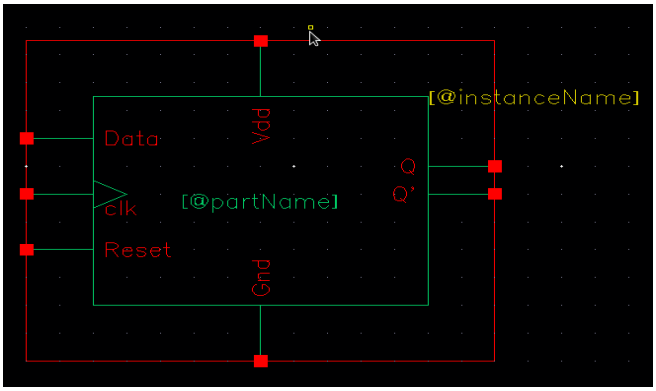

Fig. 4. Symbol of D flip flop with synchronous reset.

V. TRANSIENT RESPONSE ANALYSIS

Transient response analysis for a D flip-flop with synchronous reset involves simulating and analyzing the flip-flop's output behavior in response to changes in input data and reset signals over time, ensuring correct operation during transitions [10].

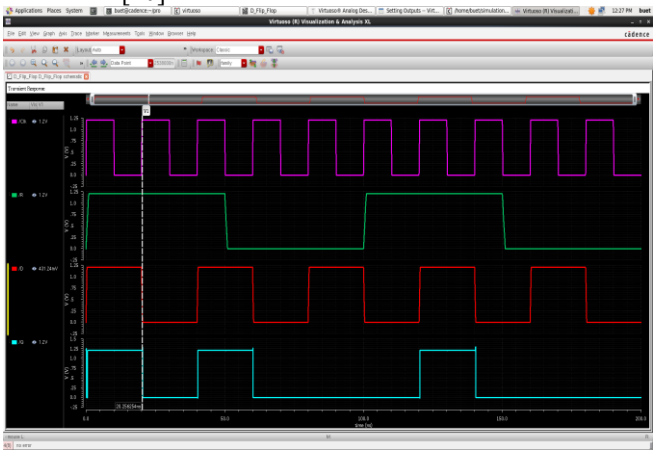

Fig. 5. Transient Response when the reset value is high

In the figure-4; the reset value is high so the output follows the input at v1 vertical line.

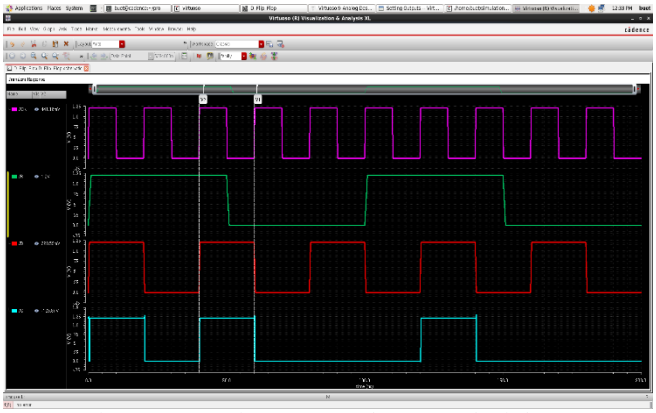

Fig. 6. Transient response when reset value is low.

In the figure-5; we have seen that the reset value is low before the clock pulse arrived but the output will not change until the next positive clock signal. This means that the output is activated only in the positive edge.

VI. DELAY ANALYSIS

A. Propagation Delay:

Propagation delay for a D flip-flop with synchronous reset in VLSI design is the time difference between when the D input transitions to 50% of its final value and when the Q output reaches 50% of its final value, indicating how quickly the flip-flop responds to changes in input data.

For the D flip flop with synchronous reset we found propagation delay of 330.1E-12 seconds. The propagation delay value of 330.1E-12 seconds indicates a delay of 330.1 picoseconds (ps), signifying the time required for the output of the D flip-flop to transition in response to changes at its input [11].

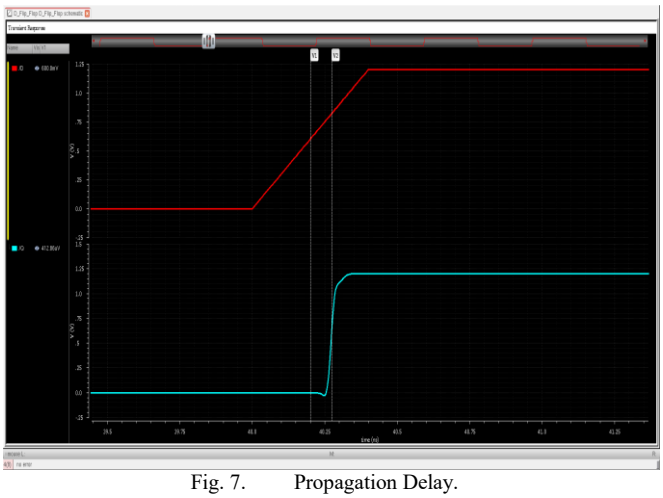

Fig. 7. Propagation Delay.

B. Rise Time:

The rise time of D flip flop with synchronous reset is 21.56E-12 seconds. It indicates the duration it takes for the output signal to transition from 10% to 90% of its final value after a rising edge occurs on the clock signal, showing how quickly the flip-flop changes state in response to inputs [12].

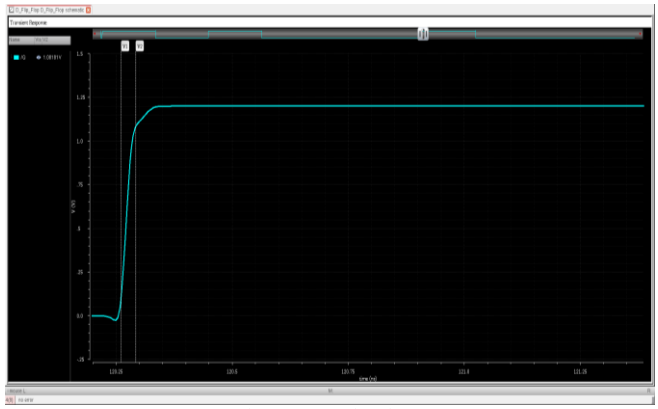

Fig. 8. Rise time

C. Fall Time:

The rise time of D flip flop with synchronous reset is 22.51E-12 seconds. It refers to the duration it takes for the output signal to transition from 90% to 10% of its final value after a falling edge occurs on the clock signal [12].

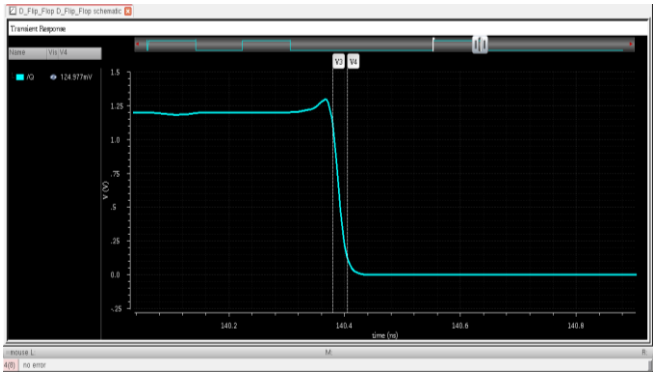

Fig. 9. Fall time

VII. Average Power Consumption

The average power consumption for a D flip-flop with synchronous reset is 594.4E-9 watts. It means that on average, the flip-flop consumes 594.4 nanowatts (nW) of electrical power during its normal operation. This metric reflects the rate at which energy is expended or dissipated by the flip-flop over time, encompassing both static (leakage) and dynamic (switching) power components.

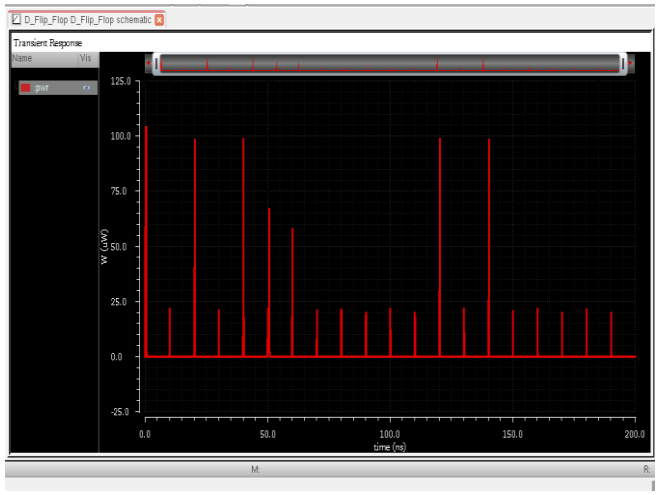

Fig. 10. Average power consumption

VIII. Noise Analysis

A. Input Noise:

In the input noise graph, the higher input noise at lower frequencies for a D flip-flop with synchronous reset is due to noise sources such as thermal and flicker noise having longer periods to influence the signal, causing greater interference. At higher frequencies, the shorter clock cycles minimize the duration during which noise can affect the signal, and the circuit's filtering mechanisms become more efficient [13].

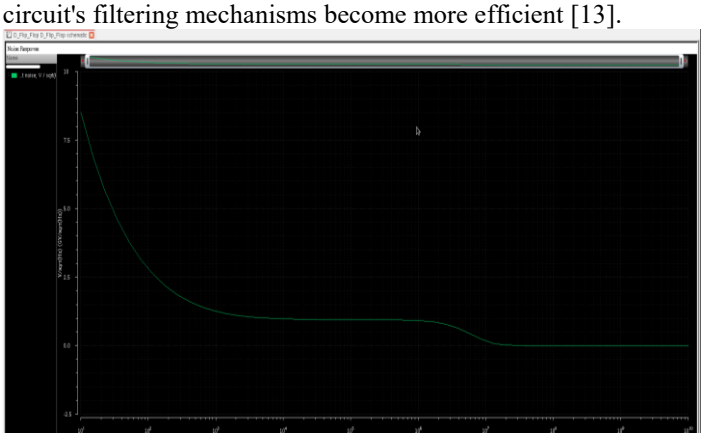

Fig. 11. Observed input noise

B. Output Noise:

In the output noise graph, the higher noise at lower frequencies for a D flip-flop with synchronous reset is due to prolonged exposure to noise sources like thermal and flicker noise during slower clock cycles, leading to increased signal instability. Conversely, at higher frequencies, shorter clock cycles minimize noise impact, while improved circuit filtering effectively reduces noise levels, resulting in a clearer output signal. Thus, frequency-dependent noise characteristics and enhanced filtering contribute to the observed noise behavior in the flip-flop [14].

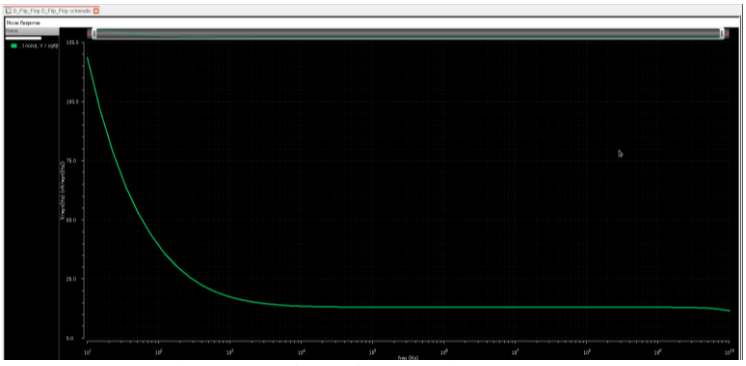

Fig. 12. Observed output noise

IX. Layout Design

A. Cell Layout:

The cell layout of a D flip-flop with synchronous reset refers to the physical arrangement of transistors, interconnects, and other components on a semiconductor substrate to implement the flip-flop circuit. This layout includes the precise positioning and connections of these elements according to the design specifications and constraints [15].

After doing the DRC and LVS test the cell layout with minimum blocks of the d flip flop with synchronous reset is-

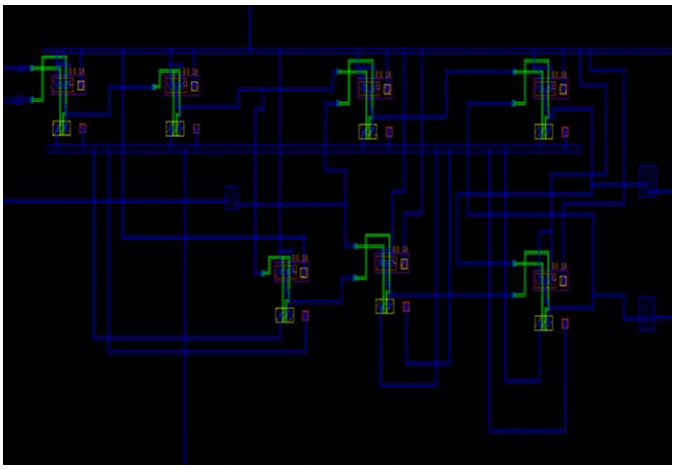

Fig. 13. Cell layout design with minimum blocks

B. Chip layout with I/O pad placement:

Chip layout with I/O pad placement for a D flip-flop with synchronous reset involves strategically arranging circuit components to optimize performance and minimize noise. It includes positioning the flip-flop, routing reset signals, and placing I/O pads for efficient signal connectivity and manufacturability in semiconductor fabrication.

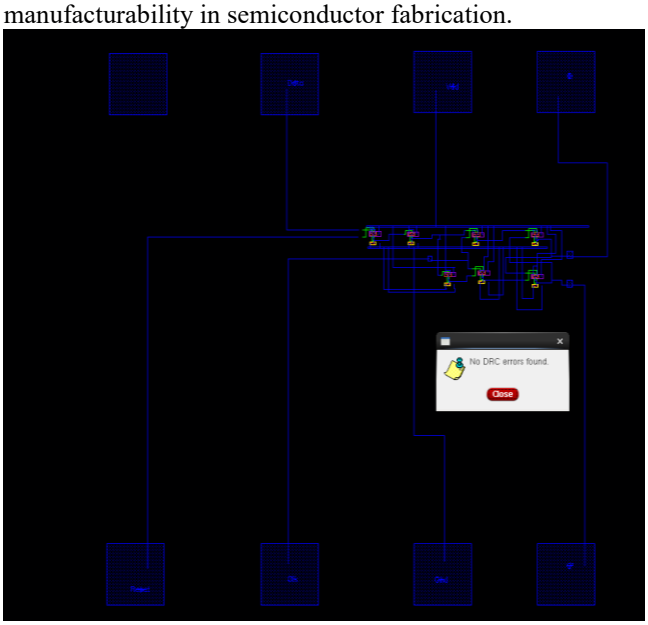

Fig. 14. Chip layout with I/O pads.

X. CONCLUSION

In conclusion, the study of the D flip-flop with synchronous reset has yielded significant insights into its design, performance, and practical implications in modern digital circuitry. By incorporating synchronous reset capability, the flip-flop ensures precise and synchronized resetting of stored data, enhancing overall reliability and operational predictability.

Through rigorous simulations and theoretical analyses, critical performance metrics such as setup time, hold time, propagation delay, and average power consumption were meticulously evaluated. The flip-flop demonstrated a propagation delay of 330.1 picoseconds, indicating its responsiveness to input changes. It exhibited a rise time of 21.56 picoseconds and a fall time of 22.51 picoseconds, underscoring its rapid state transition capabilities. The average power consumption of 594.4 nanowatts reflects its efficiency in power utilization during operation.

Furthermore, noise analysis revealed that higher input noise at lower frequencies is mitigated at higher frequencies due to improved circuit filtering, enhancing signal stability. The layout design, including cell layout and chip layout with optimized I/O pad placement, adhered to stringent design rules and verified through DRC and LVS tests, ensuring manufacturability and performance integrity.

This research contributes to advancing digital circuit design by demonstrating the efficacy of synchronous reset in enhancing data integrity and operational robustness. Future directions could explore further optimization of power efficiency and noise reduction techniques, as well as the integration of advanced materials and technologies to push the boundaries of flip-flop performance. Ultimately, the D flip-flop with synchronous reset represents a pivotal advancement in digital system architecture, promising more reliable and efficient computing solutions for diverse applications in technology and industry.

REFERENCES

[1] GeeksforGeeks, “Introduction of Sequential Circuits.” Accessed: Jun. 24, 2024. [Online]. Available: https://www.geeksforgeeks.org/introduction-of-sequential-circuits/

[2] Electronics for you, “Flip-Flop Types, Truth Table, Circuit, Working, Applications.” Accessed: Jun. 24, 2024. [Online]. Available: https://www.electronicsforu.com/technology-trends/learn-electronics/flip-flop-rs-jk-t-d

[3] Intel, “Re_ Sync Resets with Clock Enables - Intel Community.” Accessed: Jun. 24, 2024. [Online]. Available: https://community.intel.com/t5/Programmable-Devices/Sync-Resets-with-Clock-Enables/m-p/1566387

[4] K. Srilatha | B. Pujitha | M. V. Sirisha, “Implementation of D Flip Flop using CMOS Technology,” *Int. J. Trend Sci. Res. Dev.*, vol. 4, no. 3, pp. 624–626, 2020, [Online]. Available: http://www.ijtsrd.com/papers/ijtsrd30554.pdf%0Ahttps://www.ijtsrd.com/engineering/electronics-and-communication-engineering/30554/implementation-of-d-flipflop-using-cmos-technology/k-srilatha

[5] N. K. Kaphungkui, “Design of low-power , high performance flip-flops,” no. February, 2019, doi: 10.6088/ijaser.030400014.

[6] Cadence, “high frequency D flip flop for phase detector.” Accessed: Jun. 24, 2024. [Online]. Available: https://community.cadence.com/cadence_technology_forums/f/rf-design/42223/high-frequency-d-flip-flop-for-phase-detector

[7] Electronics tutorial, “The D-type Flip Flop.”

Accessed: Jun. 24, 2024. [Online]. Available: https://www.electronics-tutorials.ws/sequential/seq_4.html

[8] Electronics tutorial, “Sequential Logic Circuits and the SR Flip-flop.” Accessed: Jun. 24, 2024. [Online]. Available: https://www.electronics-tutorials.ws/sequential/seq_1.html

[9] D. K. Pham, “Design of schematic synchronously clocked JK flip-flop using CMOS technology,” no. April, pp. 27–30, 2021.

[10] I. V Beverte, “flip flops,” vol. 0, no. 4, pp. 463–470, 1992, [Online]. Available: https://doi.org/10.1016/B978-075064582-9/50007-X

[11] C. Vlsi, “Introduction to,” USA, 2018. [Online]. Available: https://www3.nd.edu/~kogge/courses/cse40462-VLSI-fa18/www/Public/Lectures/Delay-A.pdf

[12] Pichotech, “Rise and fall time measurements,” Pico Technology. Accessed: Jun. 24, 2024. [Online]. Available: https://www.picotech.com/library/oscilloscopes/rise-time

[13] R. Oshana, “Introduction to Digital Signal Processing,” *DSP Embed. Real-Time Syst.*, pp. 1–14, 2012, doi: 10.1016/B978-0-12-386535-9.00001-9.

[14] Overflow Stack, “synchronous-vs-asynchronous-resets-in-fpga-system.” Accessed: Jun. 24, 2024. [Online]. Available: https://stackoverflow.com/questions/34067276/synchronous-vs-asynchronous-resets-in-fpga-system

[15] H. Beach, “(12) United States Patent (10) Patent No .:,” vol. 1, no. 12, 2001, [Online]. Available: https://patentimages.storage.googleapis.com/b4/ec/32/4b38499bb21f49/US6333656.pdf